memory cell being coupled to a gate line and a data line that cross at the memory cell, wherein a memory cell comprises:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal, wherein the gate insulator includes a conductive path;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

Please add new claims 26-31 as follows:

26. (New) A memory cell, comprising:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal, wherein the gate insulator includes a portion of the diffusive metal;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

27. (New) The memory cell of claim 26, wherein the channel region, the source, and the drain are parts of a continuous layer of semiconductor material.

28. (New) The memory cell of claim 27, wherein the source and drain are doped regions of the layer of semiconductor material.

29. (New) The memory cell of claim 26, wherein the gate insulator extends between the diffusive metal and the floating gate, and between the floating gate and the channel region.

30. (New) The memory cell of claim 29, wherein the diffusive metal is a gate electrode.

31. (New) The memory cell of claim 26, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.